IN THE CLAIMS

1. (Currently Amended) A stack package including two or more area array type chip scale packages, each chip scale package comprising:

a substrate;

a plurality of ball land pads formed on a lower surface of the substrate;

a plurality of circuit patterns terminating in a plurality of connection pads formed outside the area in which the ball land pads are formed, the circuit patterns and the plurality of connection pads formed on the lower surface of the substrate and electrically connected to the ball land pads; and

one or more chips installed on an upper surface of the substrate and electrically connected to the circuit patterns,

wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other in a manner where the ball land pads of the upper stacked chip scale package face the opposite direction as the ball land pads of the lower stacked chip scale packages, and wherein the circuit patterns on the lower surface of the substrate of the upper stacked chip scale package are electrically connected to the circuit patterns on the lower surface of the substrate of the lower stacked chip scale package by ends of stack package side-connecting boards ~~attached to~~ having wiring patterns electrically connected to the plurality of connection pads of the circuit patterns on the lower surface of the substrate on the upper stacked chip and to the plurality of the connection pads of the circuit patterns on the lower surface of the substrate of the lower stacked chip.

2. (Previously cancelled)

2 ~~3.~~ (Currently Amended) The stack package according to claim 1, wherein each connecting board comprises a flexible film ~~and~~ with the wiring patterns formed on the film.

3 ~~4.~~ (Original) The stack package according to claim 1, wherein a hole is formed in the substrate of each chip scale package, and the chip is electrically connected to the circuit patterns by bonding wires passing through the hole.

4 ~~5.~~ (Original) The stack package according to claim 3, wherein a plurality of bonding pads of each chip scale package are formed on the central region of the chip and

exposed through the hole, and wherein one end of each bonding wire is attached to a corresponding bonding pad of the chip.

5 ~~6.~~ (Original) The stack package according to claim ~~3~~ 4, wherein the chip is protected by a first encapsulating part, and the bonding pads and the bonding wires are protected by a second encapsulating part.

6 ~~7.~~ (Original) The stack package according to claim ~~6~~ 5, wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other by an adhesive applied on the first encapsulating part.

7 ~~8.~~ (Original) The stack package according to claim 1, wherein a plurality of solder balls is formed on the ball land pads of the lowest stacked chip scale package.

8 ~~9.~~ (Original) The stack package according to claim 1, wherein a single chip scale package is stacked on, and electrically connected through a plurality of solder balls to adjacently stacked chip scale packages coupled by connecting boards.

9 ~~10.~~ (Original) The stack package according to claim 1, wherein an adjacently stacked chip scale packages coupled by connecting boards are stacked on, and electrically connected through a plurality of solder balls to another adjacently stacked chip scale packages coupled by connecting boards.

11. (Cancelled)

12. (Cancelled)

10 ~~13.~~ (Currently Amended) The stack package according to claim ~~12~~ 9, wherein both ends of the connecting board at which the connecting board is attached to the connection pads are bent.

14-20. (Cancelled)

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~~21.~~ (Currently Amended) A stack package comprising:

a first area array type chip scale package having a substrate that defines first and second sides of the first chip scale package, the second sides opposite the first sides, a first matrix of ball land pads within a defined first area, ~~and~~ one or more chips installed on an upper surface of the substrate, and a plurality of first connection pads outside the defined first area near the first and second sides of the chip scale package, the first chip scale package including a first circuit pattern formed on a lower surface of the substrate, the first circuit pattern electrically connected to the plurality of first connection pads; and

a second area array type chip scale package having a substrate that defines first and second sides of the second chip scale package, the second sides opposite the first sides, a second matrix of ball land pads within a defined second area, ~~and~~ one or more chips installed on an upper surface of the substrate, and a plurality of second connection pads outside the defined second area near the first and second sides of the chip scale package, the first chip scale package including a second circuit pattern formed on a lower surface of the substrate, the second circuit pattern electrically connected to the plurality of second connection pads,

wherein the lower surfaces of the substrates of the chip scale packages face the opposite direction, and

wherein ~~the first matrix of ball land pads is the same size as the second matrix of ball land pads~~ the plurality of first connection pads and the plurality of second connection pads are electrically connected with one another via connecting boards attached to the first and second sides of the first and second chip scale packages.

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~~22.~~ (Currently Amended) The stack package of claim ~~21~~, wherein ~~each chip scale package includes a circuit pattern formed on the lower surface of the substrate that is electrically connected to the ball land pads, and~~

~~The circuit patterns on the two chip scale packages are electrically connected~~ wherein the first matrix of ball land pads is substantially the same size as the second matrix of ball land pads.

23. (Cancelled)

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~~24.~~ (Currently Amended) The stack package of claim ~~21~~, further comprising a plurality of solder balls formed only on the ball land pads of the first chip scale package.

14 25. (Previously presented) The stack package of claim 13, further comprising a third chip scale package having a third matrix of ball land pads the same size as the first and second matrices of ball land pads,

wherein the third chip scale package is electrically connected to the ball land pads of the second chip scale package through a plurality of solder balls formed on the third matrix of ball land pads on a lower surface of a substrate of the third chip scale package.

15 26. (Previously presented) The stack package of claim 13, further comprising:

a third chip scale package having a substrate, a third matrix of ball land pads and one or more chips installed on a lower surface of the substrate; and

a fourth chip scale package having a substrate, a fourth matrix of ball land pads and one or more chips installed on a lower surface of the substrate,

wherein the lower surfaces of the substrates of the third and fourth chip scale packages face the opposite direction,

wherein the third and fourth matrices of ball land pads are the same size as the first and second matrices of ball land pads, and

wherein the third chip scale package is electrically connected to the ball land pads of the second chip scale package through a plurality of solder balls formed on the third matrix of ball land pads of the third chip scale package.

16 27. (New) A stack package including two or more area array type chip scale packages, each chip scale package comprising:

a substrate;

a plurality of ball land pads formed on a lower surface of the substrate;

a plurality of circuit patterns formed on the lower surface of the substrate and electrically connected to the ball land pads;

a plurality of connection pads formed on the outside of the region of the substrate on which the plurality of ball land pads are formed, the plurality of connection pads electrically connected to the circuit patterns; and

one or more chips installed on an upper surface of the substrate and electrically connected to the circuit patterns,

wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other in a manner where the ball land pads of the upper stacked chip scale

package face the opposite direction as the ball land pads of the lower stacked chip scale packages, and wherein the circuit patterns on the lower surface of the substrate of the upper stacked chip scale package are electrically connected to the circuit patterns on the lower surface of the substrate of the lower stacked chip scale package by connecting boards electrically connected through the connection pads to the circuit patterns on the lower surface of the substrate on the upper stacked chip and through the connection pads to the circuit patterns on the lower surface of the substrate of the lower stacked chip.

17 ~~28.~~ (New) The stack package according to claim ~~27~~ 16, wherein both ends of the connecting board adjacent the connecting board attachment to the connection pads are bent so that the connecting board extends around the sides of the chip scale package.

18 ~~29.~~ (New) The stack package according to claim ~~28~~ 17, wherein the bent-ends connecting board is generally C-shaped.

19 ~~30.~~ (New) A stackable stack package comprising:

a first chip scale package including a first substrate, the first substrate having one or more first chips on a first surface of the first substrate, the first substrate further having one or more first ball land pads within a given first area on an opposite surface of the first substrate, the first substrate further having a plurality of first circuit patterns connecting the one or more first chips to the one or more ball land pads, the plurality of first circuit patterns terminating outside the given area in a plurality of first connection pads;

a second chip scale package including a second substrate, the second substrate having one or more second chips on a first surface of the second substrate, the second substrate further having one or more second ball land pads within a second given area on an opposite surface of the second substrate, the second substrate further having a plurality of second circuit patterns connecting the one or more second chips to the one or more second ball land pads, the plurality of second circuit patterns terminating outside the given second area in a plurality of second connection pads;

the first and the second chip scale packages facing opposite directions from one another in a stack, the first and the second chip scale packages being interconnected by one or more connecting boards extending between and electrically connecting the plurality of first connection pads with the plurality of second connection pads.

20 ~~31.~~ (New) The stackable stack package of claim ~~30~~ 19 which further comprises:

one or more solder balls formed only on the one or more first ball land pads, thereby leaving exposed the one or more second ball land pads for stacking of one or more solder ball-equipped chip scale packages thereon.

21 ~~32.~~ (New) The stackable stack package of claim ~~31~~ 20, wherein there are two or more such stackable stack packages configured in a stack with the one or more solder balls of one such stackable stack package directly connected to the one or more exposed second ball land pads of another such stackable stack package.

22 ~~33.~~ (New) The stackable stack package of claim ~~31~~ 20, wherein inner surfaces of the one or more first and the one or more second chips inwardly face one another, which further comprises:

first and second encapsulants protecting the inner surfaces of the one or more first and second chips; and

an adhesive layer adhering together the first and second encapsulants and the encapsulated one or more first and second chips.

23 ~~34.~~ (New) The stackable stack package of claim ~~33~~ 22, wherein the one or more connecting boards each includes a flexible film and wiring patterns formed on the film, the one or more connecting boards extending around the sides of the first and second substrates, bent ends of the one or more connecting boards extending inwardly along the opposite surfaces of the first and second substrates only outside the given area to the plurality of first and second connection pads.